o Please replace the paragraph at page 3, lines 4-14, with the following amended text:

Incidentally, when the memory cell operates, and when in a state of the electrons being held by the floating gate, a positive bias is applied to the control gate 6. It is known that a large leak current flows to the silicon nitride layer through the trap level by hole conduction. Accordingly, supposing that the control gate 6 is provided directly on the silicon nitride layer 5b, the holes from the control gate 6 are injected, and therefore a dielectric strength is unable to be kept well. The silicon oxide layer 5c is provided upward in order to restrain the holes from being injected from the control gate 6.

IN THE CLAIMS:

o Please cancel claims 9-18.

o Please add the following new claims 19-32:

19. (New) A method of manufacturing a non-volatile semiconductor memory device, the method comprising:

providing a semiconductor substrate; and

forming a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer insulating layer, the inter-layer insulating layer having a stacked film structure with at least two film layers including a silicon oxide film layer and a silicon nitride film layer;

wherein said silicon nitride film layer is formed by a JVD method.

20. (New) The manufacturing method of claim 19, wherein said JVD method includes obtaining active Si and N by plasma-decomposing at least a silane-series gas and a gas containing nitrogen.

21. (New) The manufacturing method of claim 19, wherein said inter-layer insulating layer is formed by:

depositing a silicon oxide layer on the floating gate; and

depositing a silicon nitride layer on the silicon oxide layer under the control gate.

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22. (New) The manufacturing method of claim 19, wherein said inter-layer insulating layer is formed by:

depositing a first silicon nitride layer on the floating gate;

depositing a silicon oxide layer on the first silicon nitride layer; and

depositing a second silicon nitride layer on the silicon oxide layer under the control gate;

wherein said first and second silicon nitride layers are formed by a JVD method.

23. (New) The manufacturing method of claim 19:

wherein the inter-layer insulating layer includes at least a silicon oxide layer and at least two silicon nitride layers; and

wherein at least one of the silicon nitride layers is formed by a low pressure CVD method.

24. (New) The manufacturing method of claim 19:

wherein the inter-layer insulating layer includes at least one silicon oxide layer and at least two silicon nitride layers; and

wherein at least one of the silicon nitride layers has a concentration of hydrogen on the order of $10^{21}/cm^3$ or more.

25. (New) The manufacturing method of claim 20:

wherein the inter-layer insulating layer includes at least one silicon oxide layer and at least three silicon nitride layers; and

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wherein at least one of the silicon nitride layers is provided by a low pressure CVD method.

26. (New) The manufacturing method of claim 20:

wherein the inter-layer insulating layer includes at least one silicon oxide layer and at least three silicon nitride layers; and

wherein at least one of the silicon nitride layers has a concentration of hydrogen on the order of $10^{21}/cm^3$ or more.

27. (New) A method of manufacturing a non-volatile semiconductor memory device, the method comprising:

providing a semiconductor substrate; and

forming a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer insulating layer having a stacked film structure with at least three film layers including a silicon oxide film layer and a silicon nitride film layer;

wherein said silicon nitride film layer has a concentration of hydrogen on the order of $10^{19}/cm^3$ or less.

28. (New) The manufacturing method of claim 27:

wherein the silicon nitride layer with a concentration of hydrogen on the order of $10^{19}/cm^3$ or less is stacked adjacent to at least one of the upper surface of the floating gate and the lower surface of the control gate.

29. (New) The manufacturing method of claim 27:

wherein the inter-layer insulating layer includes at least one silicon oxide layer and at least three silicon nitride layers; and

wherein at least one of the silicon nitride layers is formed by a low pressure CVD method.

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30. (New) The manufacturing method of claim 29:

wherein the silicon nitride layer formed by the low pressure CVD method is sandwiched between other layers of the inter-layer insulating layer.

31. (New) The manufacturing method of claim 27:

wherein the inter-layer insulating layer includes at least one silicon oxide layer and at least three silicon nitride layers; and

wherein at least one of the silicon nitride layers has a concentration of hydrogen on the order of $10^{21}/cm^3$ or more.

32. (New) The manufacturing method of claim 31:

wherein at least one of the silicon nitride layers with a concentration of hydrogen on the order of $10^{21}/cm^3$ or more is sandwiched between other layers of the inter-layer insulating layer.